

ABSTRACT OF THE DISCLOSURE

[0077] An embodiment of a ultra low-power data retention latch circuit involves a slave latch SL that concurrently latches the same data that is loaded into a main circuit (such as a main latch ML) during normal operation. When the circuit enters a low power (data retention) mode, power (VCC) to the main latch ML is removed and the slave latch SL retains the most recent data (retained data SA, SA-). When power is being restored to the main latch ML, the slave latch's retained data SA, SA- is quickly restored to the main latch ML through what constitute Set and Reset inputs SAR, SAR- of the ML. This arrangement ensures that data restoration is much quicker than conventional arrangements that require the output data path DATA- to be stabilized before power is re-applied to the main latch. Further, there is no need to wait for power to the ML to be stable before restoring data from the SL to the ML, providing an increase in data restoration speed over conventional data retention latches. Using retained data SA, SA- (as mirrored in SAR, SAR-) to control the Set and Reset inputs prevents data contention in the main latch ML. Moreover, compared to known arrangements, the arrangement provides minimal loading on the DATA, DATA- output paths (driving only N7, N8), thus not compromising speed on the data path (DATAIN ... DATA/DATA-) through the main latch during normal operation.